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10/778,030	02/17/2004	Hiroshi Hamasaki	249025US2SRD	6187

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EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 07/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application Nc.	Applicant(s)
	10/778,030	HAMASAKI ET AL.
	Examiner	Art Unit
	John B. Vigushin	2841

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *13 and 14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5* is/are rejected.

7)☒ Claim(s) *4 and 6-12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *See item #6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *See Continuation Sheet*.

Continuation of Attachment(s) 6). Other: Definition and examples of LSI on Internet (GOOGLE) (one sheet); English language translation of paragraph [0021] of JP08-097352 A (one sheet); IDS PTO-1449//01 Mar 2006 (Paper #0306); IDS PTO-1449//10 Jan 2006 (Paper #0106); IDS PTO-1449//17 Feb 2004 (Paper #0204); Related Case List//19 Dec 2005 (Paper #1205); Related Case List//10 Nov 2005 (Paper #1105); Related Case List//13 Jun 2005 (Paper No. 0605); Related Case List//03 Mar 2005 (Paper #0305).

DETAILED ACTION

Election/Restrictions

1. Claims 13-14 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention (Group II), there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on May 11, 2006.

2. Applicant's election with traverse of product Claims 1-12 in the reply filed on May 11, 2006 is acknowledged. The traversal is on the ground(s) that the search for the claimed subject matter of Groups I and II "would have to be searched in a handful of sub-classes" and that "since electronic searching is commonly performed, a search may be made of a large number of, or theoretically all, subclasses without substantial additional effort and therefore "a search and examination of the entire application would not place a *serious* burden on the Examiner." This is not found persuasive.

The number of class/subclasses and the availability of electronic search engines for conducting a prior art search are not the criteria for determining burden. In the instant case, the criteria for proper restriction are to show that the inventions of Group I and Group II are distinct and that they have acquired a separate status in the art. This has been properly done in the Examiner's Restriction of April 11, 2006, on p.2, sections 2 and 3. In that Restriction, Groups I and II were shown to be distinct inventions (section 2) and that the search required for Group II (process Claims 13-14) is not required for Group I (product Claims 1-12) (section 3). Specifically, the search for the process step in Group II of pushing the heat conductive material layer to have an appropriate

thickness is not required for the search of a LSI package arranged on a mounting board of Group I.

Furthermore, the Applicant has failed to provide an explanation as to why the product Claims 1-12 of Group I and the process Claims 13-14 of Group II are not distinct inventions as established by the Examiner, which is required for a proper traversal.

The requirement is still deemed proper and is therefore made FINAL.

Claim Objections

3. Claims 2 and 12 are objected to because of the following informalities:

In Claim 2, line 4: "is" should be changed to --are--.

In Claim 12, line 3: "waveguides" should be changed to --waveguide--.

Appropriate correction is required.

Rejections Based On Prior Art

4. The following references were relied upon for the rejections hereinbelow:

Yamamoto (JP08-097352 A)† Islam (US 6,954,084 B2)

Byers et al. (US 6,906,407 B2)

Definition and examples of LSI devices found on the Internet (one sheet).

†Made of record by the Applicant in IDS filed January 10, 2006.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> **(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.**

6. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Byers et al. in conjunction with Islam for providing enabling evidence that field programmable gate arrays (FPGA) are a species of Large Scale Integrated (LSI) circuits, in accordance with the practice of multiple-reference 35 USC § 102 rejections (see MPEP § 2131.01).

As to Claim 1, Byers et al. discloses, in Fig. 4, an LSI package 300 arranged on a mounting board 106, comprising: a field programmable gate array (FPGA) IC 10--which is a type of LSI, as taught in *Islam (col.2: 9-12)*, and hereinafter will be referred to as LSI 10--configured to process signals, the LSI 10 having signal input and output terminals 11 (col.2: 37-43); an interposer (package 107 of IC device 102) configured to mount LSI 10, and including first signal terminals electrically connected to the signal input and output terminals 11 of LSI 10 (col.4: 1-7), second electric terminals (conductive pads; col.3: 53-54) for electrically connecting the LSI 10 to the mounting board 106 (col.3: 45-49), internal wirings (i.e., the I/O wires routed within the multiple wiring layers, col.4: 5-7, and additional internal wiring 130, col.4: 12-15) electrically connected to the first signal

terminals (col.4: 5-7), and first coupling parts 316 connected to the internal wirings 130 (Fig. 4; col.5: 39-40); and an interface module (package 111 of IC device 104) including signal transmission lines--i.e.,optical fibers, not shown, but disclosed as a component of IC device 104 that provides optical device functionality to IC device 104 and is connected to I/O connector 320, said I/O connector 320 receiving a peripheral component that accesses the optical functionality of optical IC device 104 through the transmission lines (col.5: 41-45)--configured to transmit the signals to outside and receive the signals from outside (by means of I/O connector 320; col.3: 13-19 and col.5: 41-45) and second coupling parts 314 (col.5: 34-37) electrically connected to the transmission line (through the wiring 140 which leads to IC chip 120 which leads to the connections disclosed between IC chip 120 and the optical transmission line fibers; col.5: 34-45), the second coupling parts 314 being electrically connected to the first coupling parts 316 by means of mechanical contact, respectively (col.5: 31-40).

As to Claim 2, Byers et al. further discloses the interposer 107 has front (entire upper surface inclusive of cavity surface for LSI 10 and surface for carrying first coupling parts 316) and rear (bottom) surfaces opposed to each other; the LSI 10 and the first coupling parts 316 are mounted on the front surface of the interposer 107 and the second electrical terminal is provided on the rear surface of the interposer; and the interface module 111 further includes an I/O element--i.e., IC 120--configured to output the signals to the optical fiber transmission line and to input the signals from the optical fiber transmission line (col.3: 15-19; col.5: 41-44), the second coupling parts 314 electrically connected to the input-output element IC 120 (Fig. 4; col.5: 36-37).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of: 1) a definition of LSI with examples, as found on the Internet; and 2) Byers et al. *Examiner's Note*: The machine English equivalent of paragraph [0021] from the Japanese Patent Office is not entirely clear regarding a specific gap height between interposer and interface module based on the pins. For this reason, the Examiner's interpretation of the meaning of paragraph [0021] in Yamamoto used in the rejection of Claim 3, below, was determined by consultation with a USPTO official Japanese translator. The Examiner will attempt to acquire, but cannot guarantee, a

better written English translation. The Applicant is therefore requested to provide clarity and accuracy to the interpretation of paragraph [0021] with, at least, an English language translation of paragraph [0021] and any other relevant portions of the Japanese document to be included with their arguments in their Response to the present Office Action. For the record, the machine translation of paragraph [0021] will nevertheless be included by the Examiner as an attachment to the present Office Action. The remaining claim limitations rejected are believed to be sufficiently clear from Figs. 1 and 2 of the Japanese document already made of record by the Applicant.

A) As to Claim 1:

I. Yamamoto discloses, in Fig. 1, a multi-chip electronic component package, comprising: an electronic component 9 configured to process signals, the electronic part 9 having signal input and output (I/O) terminals; an interposer 2 configured to mount the electronic component 9, and including first signal terminals electrically connected to the signal I/O terminals of the electronic component 9, second electric terminals (to which bumps 8 are attached) for electrically connecting the electronic component to another level of packaging (not shown in Fig. 1), internal wirings electrically connected to the first signal terminals, and first coupling parts (pin holes; see also Fig. 2) electrically connected to the internal wirings (see also Fig. 2); and an interface module 1 including signal transmission lines (the internal signal lines electrically connected to chip 3 by bond wires and to pins 7 by vias) configured to transmit the signals to outside (i.e., to a device external to the interface module package which includes the interposer 2 by way of vias that connect to pins 7) and to receive the signals from outside (i.e., from a device

external to the interface module package which includes the interposer 2 by way of vias that connect to pins 7) and second coupling parts (pins 7) electrically connected to the transmission line (again, by way of the vias), the second coupling parts 7 being electrically connected to the first coupling parts (pin holes) by means of mechanical contact, respectively (see also Fig. 2).

IIa. Yamamoto does not identify the electronic component(s) 9 mounted on interposer 2 and does not show or, apparently, teach to what higher level of packaging the multi-chip electronic component package of Fig. 1 is mounted by way of the bumps 8.

IIb. LSI chips are old and well-known in the art, as evidenced by a definition of LSI (large-scale integrated circuits) found on the Internet (see Google™ attachment; definition highlighted in red ink). The definition includes exemplary application of LSI technology to memory chips and microprocessors.

IIc. Since Yamamoto teaches a multi-chip electronic component package, then the modification of chips 9 on interposer 2 to include LSI memory and/or microprocessor chips for high speed, high frequency applications would have been readily recognized in the pertinent art of Yamamoto, as such LSI components for applications are verifiably old and well-known in the art according to the definition. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify one or more of the electronic chips 9 on interposer 2 to be memory and/or microprocessor chips required for an application of the multi-chip electronic component package of Yamamoto.

IIIa. Byers et al. discloses an LSI package comprising an interposer 107 to which an LSI chip 10 is mounted, an interface module 111 mounted on the LSI interposer and the interposer mounted to a mounting board 106 through bumps 108 for the purpose of electrically connecting the LSI chip 10 to another level of packaging, i.e., the mounting board 106 (col.3: 43-52).

IIIb. Since both Yamamoto and Byers et al. are both in the same field of endeavor, the connection of the interposer to another level of packaging taking the form of a mounting board for electrically connecting the LSI chip, as well as the other chips and modules connected to the interposer, to a larger system board, as taught by Byers et al., would have been readily recognized in the pertinent art of Yamamoto for the same purpose as in Byers et al.

IIIc. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the interposer of the multi-chip electronic package of Yamamoto, and all chips and modules electrically connected to the interposer, to a mounting board for application to the larger electronic system on the mounting board, as taught by Byers et al.

B) As to Claim 2, modified Yamamoto further discloses, in Fig. 1: the interposer 2 has front (top) and rear (bottom) surfaces opposed to each other; the LSI 9 and the first coupling parts (pin holes) are mounted on the first surface of the interposer 2 and the second electric terminal (supporting bump 8) is provided on the rear surface of the interposer 2; and the interface module 1 further includes an input-output (I/O) element (semiconductor chip 3) configured (with bond wires 6) to output the signals to the

transmission line and to input the signals from the transmission line, the second coupling parts (pins 7) electrically connected to the I/O element 3 (by way of the vias and the transmission lines).

C) As to Claim 3:

I. Yamamoto discloses, in Fig. 1, a multi-chip electronic component package, comprising: an electronic component 9 configured to process signals, the electronic part 9 having signal input and output (I/O) terminals; an interposer 2 configured to mount the electronic component 9, and including first signal terminals electrically connected to the signal I/O terminals of the electronic component 9, second electric terminals (to which bumps 8 are attached) for electrically connecting the electronic component to another level of packaging (not shown in Fig. 1), internal wirings electrically connected to the first signal terminals, and first coupling parts (pin holes; see also Fig. 2) electrically connected to the internal wirings (see also Fig. 2); and an interface module 1 including signal transmission lines (the internal signal lines electrically connected to chip 3 by bond wires and to pins 7 by vias) configured to transmit the signals to outside (i.e., to a device external to the interface module package which includes the interposer 2 by way of vias that connect to pins 7) and to receive the signals from outside (i.e., from a device external to the interface module package which includes the interposer 2 by way of vias that connect to pins 7) and second coupling parts (pins 7) electrically connected to the transmission line (again, by way of the vias), the second coupling parts 7 being electrically connected to the first coupling parts (pin holes; see also Fig. 2), the first or second or both coupling parts being provided with a mechanism of adjusting the gap

height between the interface module 1 and the interposer 2 (Figs. 1, 2 and paragraph [0021] {see English language attachment} teach that second coupling parts--i.e., pins 7--have a predetermined height of 2.8 mm from the tip of the pin--in the pin hole--to the stop portion of the pin that lies flat on the bottom surface of interface module 1, the stop portion of pin 7 enabling the interface module to be kept at a uniform height--i.e., 2.8 mm--from the tip of the pin hence, inherently, at a uniform height from the top surface of interposer 2, thus adjusting the gap height between the interface module 1 and the interposer 2).

IIa. Yamamoto does not identify the electronic component(s) 9 mounted on interposer 2 and does not show or, apparently, teach to what higher level of packaging the multi-chip electronic component package of Fig. 1 is mounted by way of the bumps 8.

IIb. LSI chips are old and well-known in the art, as evidenced by a definition of LSI (large-scale integrated circuits) found on the Internet (see Google™ attachment). The definition includes exemplary application of LSI technology to memory chips and microprocessors.

IIc. Since Yamamoto teaches a multi-chip electronic component package, then the modification of chips 9 on interposer 2 to include LSI memory and/or microprocessor chips for high speed, high frequency applications would have been readily recognized in the pertinent art of Yamamoto, as such LSI components for applications are verifiably old and well-known in the art according to the definition. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify

one or more of the electronic chips 9 on interposer 2 to be memory and/or microprocessor chips required for an application of the multi-chip electronic component package of Yamamoto.

IIIa. Byers et al. discloses an LSI package comprising an interposer 107 to which an LSI chip 10 is mounted, an interface module 111 mounted on the LSI interposer and the interposer mounted to a mounting board 106 through bumps 108 for the purpose of electrically connecting the LSI chip 10 to another level of packaging, i.e., the mounting board 106 (col.3: 43-52).

IIIb. Since both Yamamoto and Byers et al. are both in the same field of endeavor, the connection of the interposer to another level of packaging taking the form of a mounting board for electrically connecting the LSI chip, as well as the other chips and modules connected to the interposer, to a larger system board, as taught by Byers et al., would have been readily recognized in the pertinent art of Yamamoto for the same purpose as in Byers et al.

IIIc. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the interposer of the multi-chip electronic package of Yamamoto, and all chips and modules electrically connected to the interposer, to a mounting board for application to the larger electronic system on the mounting board, as taught by Byers et al.

D) As to Claim 5, modified Yamamoto further discloses the second coupling parts include pins 7 and the first coupling parts include insertion structures (pin holes) configured to receive the coupling pins 7 and fix the coupling pins 7 (Figs. 1 and 2).

Allowable Subject Matter

10. Claims 4 and 6-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

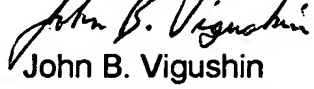
11. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
July 17, 2006